WE CLAIM:

1. An integrated circuit fabricated in the surface of a semiconductor material of a first conductivity type, said circuit having [at the surface] at least one vertical bipolar transistor surrounded at least in part by a dielectric isolation zone, said transistor comprising:

[a first surface] an emitter region of opposite conductivity type[, suitable as an emitter];

a [second surface] base contact region of said first conductivity type[, suitable as a base contact];

a well of opposite conductivity type surrounding said [first and second surface] emitter and base contact regions, extending from said surface deep into said semiconductor materia [of said first conductivity type]; and

a [layer] collector region of said opposite conductivity type buried in said semiconductor material [of said first conductivity type, suitable as collector of said transistor having sharp junctions];

a subsurface base region comprising a semiconductor band of said first conductivity type between said [layer] collector and said [surface and] emitter surrounded by said well, [said band suitable as the base of said transistor providing] having a width [controlled] determined by the [proximity] distance of said buried layer junction [to] from said surface, and a resistivity [higher] greater than the

remainder of said semiconductor material, thereby enabling said [vertical bipolar] transistor to operate [as] with a low breakdown voltage [transistor] for low ESD clamping voltage and high beta;

said [layer] collector extending laterally to said well[s], thereby electrically isolating the base and emitter [portions] of said transistor [from the remainder of] within said semiconductor material; and

[said layer] extending vertically from said surface regions, [beginning at a level] and having an upper boundary more shallow than the depth of said dielectric isolation zone, and [extending to] a lower boundary having a depth greater than the depth of said [dielectric] isolation zone, said isolation zone having a depth of 300 to 400 nm.

2. The circuit according to Claim 1 wherein said semiconductor material is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

3. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of p-type silicon in the resistivity range from about 1 to 50 Ωcm, and said emitter and buried collector are made of n-type silicon.

4. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is a semiconductor epitaxial layer.

5. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of boron, aluminum, gallium, and indium, while said regions of opposite conductivity type have a dopant species selected from a group consisting of arsenic, phosphorus, antimony, and bismuth.

6. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of n-type silicon in the resistivity range from about 5 to 50 Ωcm, and said emitter and buried collector are made of p-type silicon.

7. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of arsenic, phosphorus, antimony, bismuth, and lithium, while said regions of opposite conductivity type have a dopant species selected from a group consisting of boron, aluminum, gallium, indium, and lithium.

8. (CANCELED) The circuit according to Claim 1 wherein said electrical isolation regions have a depth of 300 to 400 μm and said buried layer has a boundary closest to said surface of less than said barrier depth.

9. A method of fabricating, in a semiconductor region of a first conductivity type having two wells of the opposite conductivity type, a vertical bipolar transistor, comprising the steps of:

depositing a photoresist layer over the surface of said region and opening a window in said layer, exposing the surface area between said wells;

implanting, at low energy, ions of the opposite

conductivity type through said window, creating a shallow layer of said opposite conductivity under said surface, suitable as the emitter of said transistor; and

implanting, at high energy and high dose, ions of said opposite conductivity type into said region of said first conductivity type through said window, creating a deep buried region having a net doping of said opposite conductivity type between, and connecting to, said wells, suitable as the collector of said transistor, and further creating a near-surface region of said first conductivity type having a doping concentration lower than that of the remainder of said region, suitable as the base of said transistor.

10. A method of fabricating, in a near-surface region of a semiconductor of a first conductivity type, a vertical bipolar transistor, comprising the steps of:

forming two nested pairs of dielectric isolation zones into said semiconductor material, the inner pair defining the lateral boundaries of said bipolar transistor, and the outer pair defining the area between wells of the opposite conductivity type;

implanting doping ions of said first or said opposite conductivity type to adjust the background doping level of the near-surface region of said semiconductor of said first conductivity type;

forming wells of said opposite conductivity type into said adjusted semiconductor material;

depositing over said surface a layer of insulating

material suitable as poly-mask dielectric, covering the area between said lateral boundaries of said transistor;

depositing a layer of poly-silicon or other conductive material onto said insulating layer;

protecting a portion of said poly-silicon and etching the remainder thereof, defining the poly-mask area between said lateral boundaries of said transistor;

depositing a first photoresist layer and opening a window therein, exposing the surface of said area between said outer isolation regions;

implanting, at low energy, ions of said opposite conductivity type into said exposed surface area, creating a shallow layer under said surface, suitable as emitter of said transistor;

implanting, at high energy and high dose, ions of said opposite conductivity type into said exposed surface area, creating a deep region under said surface having a net doping of said opposite conductivity type between, and continuous with, said wells, while further creating a band having a doping concentration of said first conductivity type lower than that of the remainder of said adjusted near-surface region;

removing said first photoresist layer;

depositing conformal insulating layers of an insulator, such as silicon nitride or silicon dioxide, over said surface and directional plasma etching said insulating layers so that only side walls around the poly-silicon dummy gate remain;

depositing a second photoresist layer and opening a

window therein, exposing the surface of said area between said outer dielectric isolation zones;

implanting, at medium energy, ions of said opposite conductivity type into said exposed surface area, creating a region of said opposite conductivity that extends to a medium depth under said surface, suitable as emitter of said transistor;

removing said second photoresist layer; and

forming a heavily doped region of said first conductivity type as contact region to said band of said first conductivity type.

11. The method according to Claim 10 further comprising the step of annealing said high energy implant at elevated temperature.

12. The method according to Claim 10 further comprising, after said step of implanting ions of said opposite conductivity type at high energy and high dose, the step of implanting, at high energy and low dose, ions of said first conductivity type for controlling the location, peak and depth of said deep region of opposite conductivity type.

13. The method according to Claim 10 comprising the modified process step of implanting said n-doping ions at high energy after said process step of implanting said n-doping ions at medium energy.

14. The method according to Claim 10 wherein said semiconductor of said first conductivity type has a peak doping concentration between 4 · 10E17 and 1 · 10E18 cm-3 after said background doping adjustment implant.

15. The method according to Claim 10 wherein said implanting of low energy ions comprises ions having an

energy suitable for creating the junction at a depth between 10 and 50 nm, and a peak concentration from about 5 · 10E17 to 5 · 10E20 cm-3.

16. The method according to Claim 10 wherein said implanting of medium energy ions comprises ions having an energy suitable for creating the junction at a depth between 50 and 200 nm, and a peak concentration from about 5 · 10E19 to 5 · 10E20 cm-3.

17. The method according to Claim 10 wherein said implanting of high energy ions of the opposite conductivity type comprises ions selected in the energy range from about 400 to 700 keV such that the peak concentration is at a different depth than that of the semiconductor of said first conductivity type, and in the dose range of about 8 · E12 to 8 · 10E13 cm-2 to overcompensate said semiconductor doping and to create a region of the opposite conductivity type at a depth of more than 200 nm.

18. The method according to Claim 12 wherein said implanting of high energy ions of said first conductivity type comprises ions selected in the energy range from about 70 to 140 keV and in the dose range of about 5 · 10E12 and 5 · 10E13 cm-2.

19. (CANCELED) The circuit according to Claim 1 further comprising an electrical connection of the emitter to the pad to be protected against ESD failure, of the base to the trigger circuit or Vss, and of the collector and well of the opposite conductivity type to Vss.